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Differences between Philips SC16C devices and Philips low power SC16CxxxB devices

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Document information

Info	Content
Keywords	UART, IrDA, Serial communications
Abstract	This application note details the differences between Philips one- and two-channel SC16Cxxx devices and Philips low power SC16CxxxB devices. Customers wishing to migrate from one Philips solution to the next can find useful information facilitating this process.

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Revision history

Rev	Date	Description
_1	20040330	Initial version (9397 750 12938).

Contact information

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1. Differences between SC16C550 and SC16C550B

Table 1: Differences between SC16C550 and SC16C550B

SC16C550	SC16C550B
Has a register called EFR. The following features are supported: auto hardware flow control using EFR bit 7 and bit 6, auto software flow control, special character select, sleep mode, XOFF interrupt, CTS and RTS interrupt, IrDA.	EFR register was removed. The following features are not supported: auto hardware flow control using EFR bit 7 and bit 6, auto software flow control, special character select, sleep mode, XOFF interrupt, CTS and RTS interrupt, IrDA.
Cannot read ISR register when LSR bit 7 is ‘1’.	ISR register can be read when LSR bit 7 is ‘1’ or ‘0’.
Clearing of the transmit empty interrupt requires a read of the ISR register and a write to TXFIFO.	Transmit empty interrupt can be cleared by reading of the ISR or a write to TXFIFO.
Does not support hardware flow control using MCR bit 5.	Support hardware flow control using MCR bit 5.
Timeout interrupt cannot be disabled with data still in the RXFIFO.	Timeout interrupt can be disabled with data in the RXFIFO.
In non-interrupt mode for LSR register to report break condition correctly the software must read ISR and LSR.	In non-interrupt mode LSR will report break condition correctly, software does not need to read ISR.
In non-interrupt mode for LSR register to report parity error correctly the software must read ISR and LSR	In non-interrupt mode LSR will report parity error correctly, software does not need to read ISR
In non-interrupt mode for LSR register to report framing error correctly the software must read ISR and LSR	In non-interrupt mode LSR will report framing error correctly, software does not need to read ISR
In FIFO mode (FCR = 0x01) and receive ready interrupt is enabled, once a character is received by the UART the software must read the LSR register first prior to reading the receive FIFO. If the software reads just the receive FIFO, then interrupt signal will remain active (logic 1).	Software can just read the receive FIFO without having to read the LSR register.
Maximum baud rate depends on the width of the write pulse (see data sheet under timing table footnote).	Maximum baud rate does not depend on the width of the write pulse.
C1 and C2 (see Figure 9 of the data sheet) recommended values are 47 pF and 100 pF.	C1 and C2 recommended values are 22 pF and 33 pF.
In DMA mode 0 the delay between back-to-back writes must be greater than X1 clock period, otherwise, the transmitter will at times miss sending out a character.	This condition is no longer applicable.
Reset signal is synchronized to X1 clock.	Reset signal is not synchronized to X1 clock.
Non-5 V tolerant pins: IOW, A0, RESET, $\overline{DCD}$	All input pins are 5 V tolerant.
Sleep Current: 1.2 mA	Sleep Current: 50 μA

2. Differences between SC16C650 and SC16C650B

Table 2: Differences between SC16C650 and SC16C650B

SC16C650	SC16C650B
This UART only supports single XON/XOFF sequence.	Supports double XON/XOFF, as well as single XON/XOFF sequence.
Cannot read ISR register when LSR bit 7 is '1'.	ISR register can be read when LSR bit 7 is '1' or '0'.
Clearing of the transmit empty interrupt requires a read of the ISR register and a write to TXFIFO.	Transmit empty interrupt can be cleared by reading of the ISR or a write to TXFIFO.
The software must fill up the transmit FIFO to transmit trigger level in one bit time, otherwise, the UART might give multiple transmit empty interrupts. This is due to the fact that the UART evaluates transmit FIFO empty condition after the start bit is sent, and if the data in the FIFO is still below the trigger level, the UART will keep generating interrupts.	The software has one character time to fill up the transmit FIFO to transmit trigger level. The UART now evaluates the transmit FIFO empty condition after the stop bit is sent and the transmit empty interrupt is only generated once—the first time the number of bytes in the transmit FIFO falls below the trigger level.
The $\overline{\text{TXRDY}}$ pin state follows the transmit trigger level, that is, it goes HIGH once the transmit FIFO is full, and goes LOW if the data in the FIFO is below the trigger level.	Once transmit FIFO is full, the $\overline{\text{TXRDY}}$ pin goes HIGH, and it goes LOW as soon as one byte is sent.
Timeout interrupt cannot be disabled with data still in the RXFIFO	Timeout interrupt can be disabled with data in the RXFIFO.
Interrupt signal on TX empty $1 \rightarrow 0$ 1 1 1 1 (bytes in TXFIFO)	Interrupt signal on TX empty $0 \rightarrow 1$ 16 8 24 30 (bytes in TXFIFO)
Interrupt signal on TX empty $1 \rightarrow 0$ 16 8 24 30 (bytes in TXFIFO)	Interrupt signal on TX empty $0 \rightarrow 1$ 15 7 23 29 (bytes in TXFIFO)
$\overline{\text{RTS}}$ hardware flow control $0 \rightarrow 1$ 16 24 28 28 (bytes in RXFIFO)	$\overline{\text{RTS}}$ hardware flow control $1 \rightarrow 0$ 1 8 16 24 (bytes in RXFIFO)
$\overline{\text{RTS}}$ hardware flow control $0 \rightarrow 1$ 8 16 24 28 (bytes in RXFIFO)	$\overline{\text{RTS}}$ hardware flow control $1 \rightarrow 0$ 0 7 15 23 (bytes in RXFIFO)
In non-interrupt mode, for LSR register to report break condition correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report break condition correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report parity error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report parity error correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report framing error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report framing error correctly; software does not need to read ISR.
In FIFO mode (FCR = 0x01) and receive ready interrupt is enabled, once a character is received by the UART the software must read the LSR register first prior to reading the receive FIFO. If the software reads just the receive FIFO, then interrupt signal will remain active (logic 1).	Software can just read the receive FIFO without having to read the LSR register.
Maximum baud rate depends on the width of the write pulse (see data sheet under timing table footnote).	Maximum baud rate does not depend on the width of the write pulse.

Table 2: Differences between SC16C650 and SC16C650B *…continued*

SC16C650	SC16C650B
C1 and C2 (see Figure 5 of the data sheet) used to be 22 pF and 33 pF; the new recommended values are 47 pF and 100 pF.	C1 and C2 recommended values are 22 pF and 33 pF.
In DMA mode 0 the delay between back-to-back writes must be greater than X1 clock period, otherwise, the transmitter sometimes will miss sending out a character.	This restriction is no longer applicable.
Reset signal is synchronized to X1 clock.	Reset signal is not synchronized to X1 clock.
Non-5 V tolerant pins: IOW, A0, RESET, $\overline{\text{DCD}}$	All input pins are 5 V tolerant.
Sleep current: 1.2 mA	Sleep current: 50 μA

3. Differences between SC16C750 and SC16C750B

Table 3: Differences between SC16C750 and SC16C750B

SC16C750	SC16C750B
Has a register called EFR that supports auto hardware flow control using EFR bit 7 and bit 6.	EFR register was removed. The following features are no longer supported: auto hardware flow control using EFR bit 7 and bit 6
Cannot read ISR register when LSR bit 7 is a '1'.	ISR register can be read when LSR bit 7 is '1' or '0'.
Clearing of the transmit empty interrupt requires a read of the ISR register and a write to TXFIFO.	Transmit empty interrupt can be cleared by reading of the ISR or a write to TXFIFO.
Does not support hardware flow control using MCR bit 5.	Support hardware flow control using MCR bit 5
Timeout interrupt cannot be disabled with data still in the RXFIFO.	Timeout interrupt can be disabled with data in the RXFIFO.
In non-interrupt mode, for LSR register to report break condition correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report break condition correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report parity error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report parity error correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report framing error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report framing error correctly; software does not need to read ISR.
In FIFO mode (FCR = 0x01) and receive ready interrupt is enabled, once a character is received by the UART the software must read the LSR register first—prior to reading the receive FIFO. If the software reads just the receive FIFO, then interrupt signal will remain active (logic 1).	Software can just read the receive FIFO without having to read the LSR register.
Maximum baud rate depends on the width of the write pulse (see data sheet under timing table footnote).	Maximum baud rate does not depend on the width of the write pulse.
C1 and C2 (see Figure 4 of the data sheet) recommended values are 47 pF and 100 pF.	C1 and C2 recommended values are 22 pF and 33 pF.
In DMA mode 0, the delay between back-to-back writes must be greater than X1 clock period, otherwise, the transmitter sometimes will miss sending out a character.	This condition is no longer applicable.
Reset signal is synchronized to X1 clock.	Reset signal is not synchronized to X1 clock.
Non-5 V tolerant pins: IOW, A0, RESET, $\overline{DCD}$.	All input pins are 5 V tolerant.
Sleep current: 1.2 mA	Sleep current: 50 μA

4. Differences between SC16C2550 and SC16C2550B

Table 4: Differences between SC16C2550 and SC16C2550B

SC16C2550	SC16C2550B
Has a register called EFR. The following features are supported: auto hardware flow control using EFR bit 7 and bit 6, auto software flow control, special character select, sleep mode, XOFF interrupt, CTS and RTS interrupt, IrDA.	EFR register was removed. The following features are no longer supported: auto hardware flow control using EFR bit 7 and bit 6, auto software flow control, special character select, sleep mode, XOFF interrupt, CTS and RTS interrupts, IrDA.
Cannot read ISR register when LSR bit 7 is a '1'.	ISR register can be read when LSR bit 7 is '1' or '0'.
Clearing of the transmit empty interrupt requires a read of the ISR register and a write to TXFIFO.	Transmit empty interrupt can be cleared by reading of the ISR or a write to TXFIFO.
Timeout interrupt cannot be disabled with data still in the RXFIFO.	Timeout interrupt can be disabled with data in the RXFIFO.
In non-interrupt mode, for LSR register to report break condition correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report break condition correctly, software does not need to read ISR.
In non-interrupt mode, for LSR register to report parity error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report parity error correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report framing error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report framing error correctly; software does not need to read ISR.
In FIFO mode (FCR = 0x01) and receive ready interrupt is enabled, once a character is received by the UART the software must read the LSR register first—prior to reading the receive FIFO. If the software reads just the receive FIFO, then interrupt signal will remain active (logic 1).	Software can just read the receive FIFO without having to read the LSR register.
Maximum baud rate depends on the width of the write pulse (see data sheet under timing table footnote).	Maximum baud rate does not depend on the width of the write pulse.
C1 and C2 (see Figure 5 of the data sheet) recommended values are 47 pF and 100 pF.	C1 and C2 recommended values are 22 pF and 33 pF.
In DMA mode 0, the delay between back-to-back writes must be greater than X1 clock period, otherwise, the transmitter sometimes will miss sending out a character.	This condition is no longer applicable.
Reset signal is synchronized to X1 clock.	Reset signal is not synchronized to X1 clock.
Non-5 V tolerant pins: $\overline{CDB}$, $\overline{RIB}$, A0, $\overline{CDA}$.	All input pins are 5 V tolerant.
Sleep current: 1.2 mA	Sleep current: 50 μA

5. Differences between SC16C2552 and SC16C2552B

Table 5: Differences between SC16C2552 and SC16C2552B

SC16C2552	SC16C2552B
Cannot read ISR register when LSR bit 7 is a '1'.	ISR register can be read with LSR bit 7 is '1' or '0'.
Clearing of the transmit empty interrupt requires a read of the ISR register and a write to TXFIFO.	Transmit empty interrupt can be cleared by reading of the ISR or a write to TXFIFO.
Timeout interrupt cannot be disabled with data still in the RXFIFO.	Timeout interrupt can be disabled with data in the RXFIFO.
In non-interrupt mode, for LSR register to report break condition correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report break condition correctly, software does not need to read ISR.
In non-interrupt mode, for LSR register to report parity error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report parity error correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report framing error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report framing error correctly; software does not need to read ISR.
In FIFO mode (FCR = 0x01) and receive ready interrupt is enabled, once a character is received by the UART the software must read the LSR register first—prior to reading the receive FIFO. If the software reads just the receive FIFO, then interrupt signal will remain active (logic 1).	Software can just read the receive FIFO without having to read the LSR register.
Maximum baud rate depends on the width of the write pulse (see data sheet under timing table footnote).	Maximum baud rate does not depend on the width of the write pulse.
C1 and C2 (see Figure 3 of the data sheet) recommended values are 47 pF and 100 pF.	C1 and C2 recommended values are 22 pF and 33 pF.
In DMA mode 0, the delay between back-to-back writes must be greater than X1 clock period, otherwise, the transmitter sometimes will miss sending out a character.	This condition is no longer applicable.
MCR bit 3 is used to control interrupt driver; this bit must be set for the interrupt to come on, otherwise the interrupt pin is 3-stated.	MCR bit 3 is used to control OP2 pin only; the interrupt driver is always enabled.
Reset signal is synchronized to X1 clock.	Reset signal is not synchronized to X1 clock.
Non-5 V tolerant pins: $\overline{IOW}$, $\overline{CDA}$.	All input pins are 5 V tolerant.
Sleep current: 1.2 mA	Sleep current: 50 μA

6. Differences between SC16C652 and SC16C652B

Table 6: Differences between SC16C652 and SC16C652B

SC16C652	SC16C652B
The UART only supports single XON/XOFF sequence.	Supports double XON/XOFF, as well as single XON/XOFF sequence.
Does not support IrDA.	Supports IrDA.
Cannot read ISR register when LSR bit 7 is '1'.	ISR register can be read when LSR bit 7 is '1' or '0'.
Clearing of the transmit empty interrupt requires a read of the ISR register and a write to TXFIFO.	Transmit empty interrupt can be cleared by reading of the ISR or a write to TXFIFO.
The software must fill up the transmit FIFO to transmit trigger level in one bit time, otherwise, the UART might give multiple transmit empty interrupts. This is due to the fact that the UART evaluates transmit FIFO empty condition after the start bit is sent, and if the data in the FIFO is still below the trigger level, the UART will keep generating interrupts.	The software has one character time to fill up the transmit FIFO to transmit trigger level. The UART now evaluates the transmit FIFO empty condition after the stop bit is sent and the transmit empty interrupt is only generated once—the first time the number of bytes in the transmit FIFO falls below the trigger level.
The $\overline{\text{TXRDY}}$ pin state follows the transmit trigger level, that is, it goes HIGH once the transmit FIFO is full, and goes LOW if the data in the FIFO is below the trigger level.	Once transmit FIFO is full, the $\overline{\text{TXRDY}}$ pin goes HIGH, and it goes LOW as soon as one byte is sent.
Timeout interrupt cannot be disabled with data still in the RXFIFO	Timeout interrupt can be disabled with data in the RXFIFO.

Interrupt signal on TX empty $1 \rightarrow 0$	Interrupt signal on TX empty $0 \rightarrow 1$	Interrupt signal on TX empty $1 \rightarrow 0$	Interrupt signal on TX empty $0 \rightarrow 1$
1	16	16	15
1	8	8	7
1	24	24	23
1	30	30	29
(bytes in TXFIFO)	(bytes in TXFIFO)	(bytes in TXFIFO)	(bytes in TXFIFO)
$\overline{\text{RTS}}$ hardware flow control $0 \rightarrow 1$	$\overline{\text{RTS}}$ hardware flow control $1 \rightarrow 0$	$\overline{\text{RTS}}$ hardware flow control $0 \rightarrow 1$	$\overline{\text{RTS}}$ hardware flow control $1 \rightarrow 0$
16	1	8	0
24	8	16	7
28	16	24	15
28	24	28	23
(bytes in RXFIFO)	(bytes in RXFIFO)	(bytes in RXFIFO)	(bytes in RXFIFO)

In non-interrupt mode, for LSR register to report break condition correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report break condition correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report parity error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report parity error correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report framing error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report framing error correctly; software does not need to read ISR.
In FIFO mode (FCR = 0x01) and receive ready interrupt is enabled, once a character is received by the UART the software must read the LSR register first prior to reading the receive FIFO. If the software reads just the receive FIFO, then interrupt signal will remain active (logic 1).	Software can just read the receive FIFO without having to read the LSR register.
Maximum baud rate depends on the width of the write pulse (see data sheet under timing table footnote).	Maximum baud rate does not depend on the width of the write pulse.

Table 6: Differences between SC16C652 and SC16C652B *…continued*

SC16C652	SC16C652B
C1 and C2 (see Figure 3 of the data sheet) recommended values are 47 pF and 100 pF.	C1 and C2 recommended values are 22 pF and 33 pF.
In DMA mode 0 the delay between back-to-back writes must be greater than X1 clock period, otherwise, the transmitter sometimes will miss sending out a character.	This condition is no longer applicable.
Reset signal is synchronized to X1 clock.	Reset signal is not synchronized to X1 clock.
Non-5 V tolerant pins: IOW, A0, RESET, $\overline{DCD}$	All input pins are 5 V tolerant.
Sleep current: 1.2 mA	Sleep current: 50 μA

7. Differences between SC16C752 and SC16C752B

Table 7: Differences between SC16C752 and SC16C752B

SC16C752	SC16C752B
The UART only supports single XON/XOFF sequence.	Supports double and single XON/XOFF sequence.
Cannot read ISR register when LSR bit 7 is a '1'.	ISR register can be read when LSR bit 7 is '1' or '0'.
Clearing of the transmit empty interrupt requires a read of the ISR register and a write to TXFIFO.	Transmit empty interrupt can be cleared by reading of the ISR or a write to TXFIFO.
The software must fill up the transmit FIFO to transmit trigger level in one bit time, otherwise, the UART might give multiple transmit empty interrupts. This is because the UART evaluates transmit FIFO empty condition after the start bit is sent, and if the data in the FIFO is still below the trigger level, the UART will keep generating interrupts.	The software has one character time to fill up the transmit FIFO to transmit trigger level. The UART now evaluates the transmit FIFO empty condition after the stop bit is sent and the transmit empty interrupt is only generated once—the first time the number of bytes in the transmit FIFO falls below the trigger level.
Timeout interrupt cannot be disabled with data still in the RXFIFO.	Timeout interrupt can be disabled with data in the RXFIFO.
In non-interrupt mode, for LSR register to report break condition correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report break condition correctly, software does not need to read ISR.
In non-interrupt mode, for LSR register to report parity error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report parity error correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report framing error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report framing error correctly; software does not need to read ISR.
In FIFO mode (FCR = 0x01) and receive ready interrupt is enabled, once a character is received by the UART the software must read the LSR register first—prior to reading the receive FIFO. If the software reads just the receive FIFO, then interrupt signal will remain active (logic 1).	Software can just read the receive FIFO without having to read the LSR register.
Maximum baud rate depends on the width of the write pulse (see data sheet under timing table footnote).	Maximum baud rate does not depend on the width of the write pulse.
C1 and C2 (see Figure 12 of the data sheet) recommended values are 47 pF and 100 pF.	C1 and C2 recommended values are 22 pF and 33 pF.
In DMA mode 0, the delay between back-to-back writes must be greater than X1 clock period, otherwise, the transmitter sometimes will miss sending out a character.	This condition is no longer applicable.
If TCR register is used for hardware or software flow control, FCR register bit[7:4] must be set to a value other than 0xC.	This restriction no longer applies.
Reset signal is synchronized to X1 clock.	Reset signal is not synchronized to X1 clock.
Non-5 V tolerant pins: $\overline{CDB}$, $\overline{RIB}$, A0, $\overline{CDA}$.	All input pins are 5 V tolerant.
Sleep current: 1.2 mA	Sleep current: 50 μA

8. What you need to know if you plan to switch from Philips SC16Cxxx to SC16CxxxB device

Table 8: Guideline for switching from SC16Cxxx to lower power SC16CxxxB devices

Function	Part number	Package	Recommended part number	Comment
550	SC16C550	N40 (DIP40) A44 (PLCC44) B48 (LQFP48)	SC16C550B or SC16C650B	If you are using the following features: HW flow control, SW flow control, or IrDA, you need to replace the SC16C550 with SC16C650B.
2550	SC16C2550	N40 (DIP40) A44 (PLCC44) B48 (LQFP48)	SC16C2550B or SC16C652B	If you are using the following features: HW flow control, SW flow control, or IrDA, you need to replace the SC16C2550 with the SC16C652B. The replacement is only available in B48 package.
2552	SC16C2552	A44 (PLCC44)	SC16C2552B	Backwards compatible to SC16C2552.
650	SC16C650	N40 (DIP40) A44 (PLCC44) B48 (LQFP48)	SC16C650B	Backwards compatible to SC16C650.[1]
652	SC16C652	B48 (LQFP48)	SC16C652B	Backwards compatible to SC16C652.[1]
750	SC16C750	A44 (PLCC44 B48 (LQFP48)	SC16C750B	Backwards compatible to SC16C750.
752	SC16C752	B48 (LQFP48)	SC16C752B	Backwards compatible to SC16C752.

[1] In very rare occasions, the TXRDY pin is used. If that is the case, a software modification is required.

9. Disclaimers

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10. Contents

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